Linrui Jiang

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EDUCATION

The University of Texas at Austin (UT Austin)

M.S. in Electrical and Computer Engineering

Expected to graduate: May 2026

University of Electronic Science and Technology of China (UESTC)

Chengdu, PR China

Austin, Unite States

B.Eng. with Merit in Electronic Science and Technology

Sept. 2020 - June 2024

• GPA: 3.95/4.00 | Weighted Average: 92/100 | Ranking: 3/158 | ECE-Only GPA: 4.00/4.00

Core Courses: Circuit Analysis and Electronic Circuit (94) | Application and Design of Digital Logic (96) Microcomputer Principle and Interface Technology (94) | Signals and Systems (99)

Advanced Programming Language Design (96) | EDA Technology (96)

PROFESSIONAL SKILLS

Programming Language: Verilog, Python, C/C++; LATEX, Java

Development Tool: Cadence, Vivado, Keil, Altium Designer; Android Studio, MATLAB

Technology Stack:

• Software: Deep Learning Algorithms, Convolutional Nerual Network

• Hardware: Digital Logic Designed, Hardware System Verification

PUBLICATION

C. Li, S. Li, L. Jiang, B. Guo, J. Zhang, Z. Ye, and Y. Lin, "Generalized Neural Radiance Field Accelerator for Edge AR/VR", Submitted to ASPLOS 2025

RESEARCH EXPERIENCE

Performance and Architecture Group @ UT Austin

Austin, Unite States

Research Assistant, Advisor: Dr. Ian Wang & Dr. Junjie Li

Aug. 2024 - Present

• High-performance Monitor and Tuning Tool Designed

Conducted performance analysis and profiling for HPC applications to identify optimization opportunities.

AIoT Smart ICs & Systems Lab @ UESTC

Chengdu, PR China

Research Intern, Advisor: Prof. Jun Zhou

Oct. 2023 - June 2024

Separable CNN for Speaker Recognition | Python

- Designed a speaker recognition algorithm with the time delay neural network (TDNN), which set up a rational residual network structure and applied a comprehensive speech dataset.
- Reduced the module's equal error rate (EER) from 14.22% to **0.196**% when full-time enrollment and verification.
- Hardware-aware Algorithms for Tape Out | Python
- Made the algorithms hardware-friendly, transferring long audio segments into shorter segments and integrating the processing results from short audio segments.
- Achieved just about 0.05% performance deterioration on the systems. (0.245% compared with 0.196%)
- Hardware Implementation for Speaker Recognition | Verilog
- Designed three sub-modules for back-end classification on the Xilinx FPGA, which are responsible for storing the vectors, calculating the paradigms and introducing them into the IP core.
- Satisfies the requirement of outputting similarity results within 1ms at 100MHz clock frequency.

Efficient & Intelligent Computing Lab @ Georgia Tech

Atlanta, Unite States May 2023 - Oct. 2023

Research Intern, Advisor: Prof. Yingyan (Celine) Lin

- A Generalized Neural Radiance Field Accelerator for Edge AR/VR | Java, C
- Proposed a measurement method for the CPU, GPU, DSP and NPU performance on the Snapdragon Mobile Platform. Implemented the framework in the Docker container and using Android Studio IDE.
- Utilized the Neural Processing SDK for AI to run neural networks on edge devices. Employed AI Engine Direct SDK to invoke Qualcomm accelerators. Applied AI Model Efficiency Tool Kit to compress algorithm models for higher efficiency and lower latency.
- Obtained positive feedback and device support from the Qualcomm QIDK and QNN Team. This work is part of an ASPLOS 2025 submission.

Nanovisualization Research Group @ King A. Univ. of Sci. & Tech. Visiting Student, Advisor: Prof. Ivan Viola

Thuwal, Saudi Arabia June 2022 - July 2022

- Algorithms Optimization in a Game Design Project | Web GPU Shading Language, Java
- Reconstructed the Chrome Dino game on Shader Editor. Designed the game for fast response and precise detection by a two-step solution for collision detection, which combines Bounding Boxes and Detailed Rectangles.
- Implemented the optimized algorithms to reduce the number of Detailed Rectangles that need to be activated. Reduced the react time from 94ms to 27ms, achieving real-time reaction. Demo

LEADERSHIP & SERVICES

Diversity Support Event

Lead Student

Chengdu, CHN Sept. 2022 - Present

 Led a peer volunteer support group to assist over 120 students (mainly underrepresented groups: Women in STEM & First-generation college students) applying to graduate programmes.

- Committed 1 to 2 hours per week to provide guidance, suggestions and mentorship with 8 partners. To date, they received offers/admission letters from prestigious universities: Stanford (\times 1), Georgia Tech (\times 1), UCSD (\times 2), UVa (\times 1) and more. [Details]

HONORS & AWARDS

Merit Graduate Scholarship, top 5%, UESTCJune 2024Excellent Student Scholarship, top 10%, UESTCDec. 2022, Dec. 2023China National Scholarship, top 1%, Ministry of Education of the PRCDec. 2022Academic Outstanding Scholarship, top 15%, School of ESEDec. 2021